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AMENDMENTS TO THE DRAWINGS:

The attached sheets of Drawings include changes to Figs. 1 and 3. These sheets, which respectively include Figs. 1 and 3, replace the original sheets including Figs. 1 and 3.

Attachment: two Replacement Sheets.

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REMARKS/ARGUMENTS

Claims 1, 2, 7, 8, and 14-17 are pending in this application. By this Amendment, Applicant AMENDS claims 1, 2, 7, 8, 14, and 15, the Title of the Invention, and the Drawings, CANCELS claims 3-6 and 9-13, and ADDS claims 16 and 17.

Support for newly added claims 16 and 17 can be found in the second Paragraph on Page 22 of Applicant's originally filed Specification, and in Fig. 3 of Applicant's originally filed Drawings.

The drawings were objected to for lacking descriptive text labels for items "160," "200," "ADP," and "FL" included in Fig. 1. The drawings were also objected to because Fig. 3 included dotted lines. Applicant submits amended Figs. 1 and 3 in which the above issues have been corrected. Applicant respectfully submits that new Figs. 1 and 3 show elements and arrangements thereof that were described in Applicant's originally filed application and thus, no new matter is introduced by the amendment to Figs. 1 and 3. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the objection to the drawings.

The Title of the Invention was objected to for allegedly failing to be indicative of the invention to which the claims are directed. Applicant has amended the Title of the Invention in the manner as suggested by the Examiner. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the objection to the Title of the Invention.

Claims 2 and 8 were rejected under 35 U.S.C. § 112, second paragraph as allegedly being indefinite due to a lack of antecedent basis. Claims 2 and 8 have been amended to correct the informalities noted by the Examiner. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 2 and 8 under 35 U.S.C. § 112, second paragraph.

The Examiner rejected claims 1-3 under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 7,236,375. Applicant has amended claim 1 to recite some of the features of originally filed dependent claims 4-6. Thus, the features presently recited in claim 1 are patentably distinct from claims 1-

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3 of U.S. Patent No. 7,236,375. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1-3 under the judicially created doctrine of obviousness type double patenting.

The Examiner rejected claims 7-9 under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 6-8 of U.S. Patent No. 7,236,375. Applicant has amended claim 7 to recite some of the features of originally filed dependent claims 10-13. Thus, the features presently recited in claim 7 are patentably distinct from claims 6-8 of U.S. Patent No. 7,236,375. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 7-9 under the judicially created doctrine of obviousness type double patenting.

Claims 1 and 2 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lin (U.S. 6,259,615). Claims 1-3 and 7-9 were rejected under 35 U.S.C. § 102(a) as being anticipated by Fukumoto et al. (JP 2004-166445). Claims 4-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of Nagahara (U.S. 5,959,857). Claims 7 and 8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of Lin et al. (U.S. 2003/0206426). Claims 10-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of Lin et al., and further in view of Nagahara. Claims 14 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of Gradzki et al. (U.S. 6,011,360).

Applicant respectfully traverses the rejections of claims 1, 2, 7, 8, 14, and 15.

Claim 1 has been amended to recite:

A DC-AC converter, comprising:
a transformer having a primary winding and at least one secondary winding;
a semiconductor switching circuit arranged to allow electric current to flow from a DC power supply through the primary winding in a first or a second direction;
a current detection circuit arranged to detect the current flowing through a load connected to the secondary winding to output a current detection signal;
a voltage detection circuit arranged to detect the voltage applied to the load to output a voltage detection signal;
a current-error signal generating circuit arranged to generate a current-error

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signal based on the current detection signal and a current reference signal;
a voltage-error signal generating circuit arranged to generate a voltage-error signal based on the voltage detection signal and a voltage reference signal;
a feedback signal formation circuit arranged to provide a feedback signal in accordance with the magnitudes of the current-error signal and voltage error signal;
a switch drive circuit arranged to provide a drive signal that switches the semiconductor switching circuit on and off in accordance with the feedback signal; and
a feedback signal control circuit arranged to change the feedback signal to reduce the electric power supplied to the load when the DC power supply voltage of the DC power supply sharply rises; wherein
the feedback signal formation circuit includes:
a current-error control transistor having a control input arranged to receive the current-error detection signal; and
a voltage-error control transistor having a control input arranged to receive the voltage-error detection signal;
the voltage-error control transistor is connected in parallel with the current-error control transistor to output the feedback signal from a node where the voltage-error control transistor is connected in parallel with the current-error control transistor;
the feedback signal control circuit includes:
a sharp-voltage-change detection circuit arranged to receive the DC power supply voltage and arranged to generate a sharp-voltage-change signal by differentiating the DC power supply voltage, the sharp-voltage-change detection circuit including a capacitor and a first resistor; and
a reduction circuit including a transistor switch arranged to receive the sharp-voltage-change signal and a second resistor, the second resistor being connected in series between the transistor switch and the current-error control transistor and in series between the transistor switch and the voltage-error control transistor.
(emphasis added)

Applicant's claim 7 recites features that are similar to the features recited in Applicant's claim 1, including the above-emphasized features.

With the unique combination and arrangement of features recited in Applicant's claim 1, including the features of "a sharp-voltage-change detection circuit arranged to receive the DC power supply voltage and arranged to generate a sharp-voltage-change signal by differentiating the DC power supply voltage, the sharp-voltage-change detection circuit including a capacitor and a first resistor" and "a reduction circuit including a transistor switch arranged to receive the sharp-voltage-change signal and a second resistor, the second resistor

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being connected in series between the transistor switch and the current-error control transistor and in series between the transistor switch and the voltage-error control transistor,” Applicant has been able to provide an inverter capable of performing constant-current control on a load connected to a secondary winding of a transformer to thereby prevent a possible overcurrent or inverter shut down caused by a sharp change in a power supply voltage (see, for example, the paragraph bridging Pages 3 and 4 of Applicant’s specification).

The Examiner alleged that each of Lin and Fukumoto et al. teaches all of the features recited in Applicant’s claim 1. More specifically, the Examiner alleged that Lin teaches “a feedback signal formation circuit (60, 40) for forming a feedback signal (output of 62) in accordance with the magnitudes of said current-error signal and voltage error signal (column 5, lines 39-42, column 8, lines 28-31),” and that Fukumoto et al. teaches “a feedback signal formation circuit (Figure 3, 235, 238) for forming a feedback signal (FB) in accordance with the magnitudes of said current-error signal (output of 211) and voltage error signal (output of 212).”

Applicant has amended claim 1 to recite the features of “a sharp-voltage-change detection circuit arranged to receive the DC power supply voltage and arranged to generate a sharp-voltage-change signal by differentiating the DC power supply voltage, the sharp-voltage-change detection circuit including a capacitor and a first resistor” and “a reduction circuit including a transistor switch arranged to receive the sharp-voltage-change signal and a second resistor, the second resistor being connected in series between the transistor switch and the current-error control transistor and in series between the transistor switch and the voltage-error control transistor.” Support for this feature is found, for example, in paragraph [0020] of Applicant’s specification and Fig. 1 of Applicant’s drawings. Applicant has also amended claim 7 to recite features similar to the above features.

Lin teaches a power converter that includes a protection circuit 60 with a feedback loop 40, as shown in Fig. 2 of Lin. However, Lin fails to teach or suggest a feedback signal control circuit, as is admitted by the Examiner in the first paragraph on page 9 of the outstanding Office

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Action. The Examiner relied upon Nagahara to teach this feature.

Nagahara teaches a power supply device including an oscillation drive circuit, as shown in Fig. 3 and discussed in Column 3, Line 38 to Column 4 Line 44 of Nagahara. In Fig. 3 of Nagahara, the comparators 20 and 24 included in the block demarcated by broken-lines operate as follows: the output voltage of the diode bridge is compared with a voltage based on V_{CC} by the comparator 20 to switch between “full-bridge operation” and “single-end push-pull and half-bridge operation.” More specifically, if the output voltage of the diode bridge is greater than the voltage level of V_{CC} , the drive circuits 17a-17d are fed with the pulse signals from the oscillation control circuit to thereby achieve “full-bridge operation.” On the other hand, if the output voltage of the diode bridge is greater than the voltage level of V_{CC} , the drive circuits 17c and 17d will be biased while the drive circuits 17a and 17b are fed with the pulse signals from the oscillation control circuit 16 to thereby achieve “single-end push-pull and half-bridge operation.” Accordingly, it is thus possible to virtually expand the range of AC input voltage in which a stable DC output voltage can be obtained.

However, the system of Nagahara and the presently claimed invention are different with respect to the signal that triggers the respective feedback controls. In Fig. 3 of Nagahara, the block including the comparators 20 and 24 operates as follows. When switching from “single-end push-pull and half-bridge operation” to “full-bridge operation,” the transistor 31 turns on to raise the frequency of the oscillation control circuit 16. Furthermore, when switching back to “single-end push-pull and half-bridge operation,” the transistor 31 turns off to decrease the frequency of the oscillation control circuit 16, as is discussed in Column 8, Lines 25-61 of Nagahara.

In the present invention, the supply voltage is monitored and the feedback signal is controlled. However, according to Nagahara, the input to oscillation control circuit 16 which is connected via the resistor 15 in Fig. 3 (which the Examiner alleged corresponds to the claimed feedback signal) is only arranged to switch between “full-bridge operation” and “single-end push-pull and half-bridge operation,” as discussed in Column 8, Lines 37-61 of Nagahara. Thus,

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Nagahara differs from the present invention with respect to the signal that triggers the respective control. Furthermore, Nagahara also fails to teach or suggest a configuration in which a resistor is connected in series between a transistor of a feedback signal formation circuit and a transistor switch of a reduction circuit as in the present invention, and thus does not teach directly reducing a feedback voltage in response to an abrupt rise in a DC supply voltage, without waiting for a variation in the current or voltage to a load in order to reduce the electric power fed to the load as recited in Applicant's claim 1 and similarly recited in Applicant's claim 7.

Fukumoto et al. teaches a DC/AC converter and its controller which include a pair of transistors 235, 238 that are arranged to adjust a feedback signal FB, as shown in Fig. 3, and discussed in paragraph [0093] of Fukumoto et al. However, Fukumoto et al. does not teach or suggest a feedback control circuit arranged to reduce power supplied to a load in response to a sharply rising power supply voltage, and it surely fails to teach or suggest the feedback control circuit including a sharp-voltage-change detection circuit and a reduction circuit as recited in Applicant's claim 1 and similarly recited in Applicant's claim 7.

Thus, Lin, Nagahara, and Fukumoto et al. each clearly fail to teach or suggest the features of "a sharp-voltage-change detection circuit arranged to receive the DC power supply voltage and arranged to generate a sharp-voltage-change signal by differentiating the DC power supply voltage, the sharp-voltage-change detection circuit including a capacitor and a first resistor" and "a reduction circuit including a transistor switch arranged to receive the sharp-voltage-change signal and a second resistor, the second resistor being connected in series between the transistor switch and the current-error control transistor and in series between the transistor switch and the voltage-error control transistor" as recited in Applicant's claim 1 and similarly recited in Applicant's claim 7.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claim 1 under 35 U.S.C. § 102(b) as being anticipated by Lin, and the rejection of claims 1 and 7 under 35 U.S.C. § 102(a) as being anticipated by Fukumoto et al.

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The Examiner further submits that any rejection of claims 1 and 7 under 35 U.S.C. § 103(a) as being unpatentable over Lin, Fukumoto et al., and/or Nagahara would also be improper at least for the reasons discussed above.

The Examiner relied upon Lin et al. and Gradzki et al. to allegedly cure the deficiencies of Lin. However, Lin et al. and Gradzki et al. also clearly fail to teach or suggest the features of "a sharp-voltage-change detection circuit arranged to receive the DC power supply voltage and arranged to generate a sharp-voltage-change signal by differentiating the DC power supply voltage, the sharp-voltage-change detection circuit including a capacitor and a first resistor" and "a reduction circuit including a transistor switch arranged to receive the sharp-voltage-change signal and a second resistor, the second resistor being connected in series between the transistor switch and the current-error control transistor and in series between the transistor switch and the voltage-error control transistor" as recited in Applicant's claim 1 and similarly recited in Applicant's claim 7. Thus, Applicant respectfully submits that Lin et al. and Gradzki et al. fail to cure the deficiencies of Lin described above.

Accordingly, Applicant respectfully submits that Lin, Nagahara, Fukumoto et al., Lin et al., and Gradzki et al., applied alone or in combination, fail to teach or suggest the unique combination and arrangement of elements recited in Applicant's claim 1 and similarly recited in Applicant's claim 7.

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1 and 7 are allowable. Claims 2, 8, and 14-17 depend upon claims 1 and 7, and are therefore allowable for at least the reasons that claims 1 and 7 are allowable.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

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The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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